CLAIMS:

1. A drive circuit for a bi-stable display (100) having pixels (Pij), the drive circuit comprises:

a driver (101, 102) for supplying drive waveforms (DWk) to the pixels (Pij) to obtain during an image update period (IUk) an update of an image presented by the pixels (Pij), and

a controller (103) for controlling the driver (101, 102) to supply, during the image update period (IUk) wherein a particular optical transition of a particular one of the pixels (Pij) is required, an associated one of the drive waveforms (DWk) to the particular one of the pixels (Pij), the associated one of the drive waveforms (DWk) comprising a sequence of a particular number of pulses (SPk), wherein consecutive ones of the pulses (SPk) of the sequence are separated by a separation period of time (SPT), the particular number of said pulses (SPk), and/or a duration of said pulses (SPk), and/or a duration of the separation period (SPT) of the associated one of the drive waveforms (DWk) being determined to obtain the particular optical transition at a desired energy of the associated one of the drive waveforms (DWk).

2. A drive circuit as claimed in claim 1, wherein the controller (103) is arranged for controlling the driver (101, 102) to supply the particular number of said pulses (SPk), and/or a duration of said pulses (SPk), and/or a duration of the separation period (SPT) of the associated one of the drive waveforms (DWk) being determined to decrease an average value of the energy of the associated one of the drive waveforms (DWk)

3. A drive circuit as claimed in claim 1, wherein the drive circuit further comprises a memory (107) for storing the drive waveforms (DWk) required for all possible optical transitions of the pixels (Pij), at least one of the drive waveforms (DWk) comprising the sequence of the particular number of pulses (SPk).

4. A drive circuit as claimed in claim 1, wherein the drive circuit further comprises an averaging circuit (104) for determining, during the image update period (IUk),

or during a sequence of image update periods (IUK), for the particular one of the pixels (Pij) an average value (AV) of the energy of the associated one of the drive waveforms (DWk), and wherein the controller (103) is arranged for receiving the average value (AV) to control the particular number of said pulses (SPk), and/or a duration of said pulses (SPk), and/or a duration of the separation period (SPT) of the associated one of the drive waveforms (DWk) in response to the average value (AV) to decrease the average value (AV).

5. A drive circuit as claimed in claim 2, wherein the controller (103) is arranged for controlling for the particular pixel (Pij) the driver (101, 102) to supply the drive waveform (DWk) comprising the particular number of pulses (SP1, ... SP6) separated by the separation period of time (SPT) as a series of sub-pulses (SSP1) during the image update period (IU2), and to supply a single pulse (DW1) only, during another image update period (IU1), the number of sub-pulses in the series (SSP1) being determined to decrease the average value (AV) of the drive waveform (DWk) during the total period in time covering the image update period (IU2) and the other image update period (IU1).

6. A drive circuit as claimed in claim 5, wherein the controller (103) is arranged for controlling for a particular pixel (Pij) the driver (101, 102) to supply the drive waveform (DWk) further comprising a shaking pulse (S1) preceding the single pulse (DW1) and/or preceding the series of sub-pulses (SSP1).

7. A drive circuit as claimed in claim 2, wherein the controller (103) is arranged for controlling for a particular pixel (Pij) the driver (101, 102) to supply during the image update period (IU21) the drive waveform (DW21) comprising the particular number of pulses (SP30, ..., SP33) separated by the separation period of time (SPT) as a series of sub-pulses (SSP4), and to supply, during another image update period (IU20), the drive waveform (DW20) comprising a single drive pulse (DP2) instead of the particular number of pulses (SP30, ..., SP33), and a reset pulse (RE2) preceding the drive pulse (DP2), the number of sub-pulses of the series (SSP4) being determined to decrease the average value (AV) of the drive waveform (DWk) during the total period in time covering the image update period (IU20) and the other image update period (IU10).

8. A drive circuit as claimed in claim 2, wherein the controller (103) is arranged for controlling for a particular pixel (Pij), the driver (101, 102) to supply, during an image

update period (IU11), the particular number of pulses (SP20, ..., SP23) separated by the separation period of time (SPT) as a series of sub-pulses (SSP3) for resetting the particular pixel (Pij) to one of its extreme optical states, and to supply during another image update period (IU10), the drive waveform (DW10) comprising a single reset pulse (RE1) instead of the series of sub-pulses (SSP3), and a drive pulse (DP1) succeeding the single reset pulse (RE1), the number of sub-pulses of the series (SSP3) being determined to decrease the average value (AV) of the energy of the drive waveform (DWk) during the total period in time covering the image update period (IU11) and the other image update period (IU10).

9. A drive circuit as claimed in claim 7 or 8, wherein the controller (103) is arranged for controlling the driver (101, 102) to supply during both the image update period (IUk) and the another image update period (IUk) a first shaking pulse (S1) preceding said reset pulse (RE1; RE2).

10. A drive circuit as claimed in claim 7 or 8, wherein the controller (103) is arranged for controlling the driver (101, 102) to supply during both the image update period (IUk) and the another image update period (IUk) a second shaking pulse (S2) occurring between said reset pulse (RE1; RE2) and the drive pulse (DP1; DP2).

11. A drive circuit as claimed in claim 1, wherein the controller (103) is arranged for controlling the driver (101, 102) to supply a level during the separation period of time (SPT) to substantially keep an optical state of the particular one of the pixels (Pij) unaltered.

12. A drive circuit as claimed in claim 1, wherein the controller (103) is arranged for controlling the driver (101, 102) to supply during the separation period (SPT) a level opposite to the level of the one of the pulses (SPk) preceding the separation period (SPT).

13. A method of driving a bi-stable display (100) having pixels (Pij), the method comprises:

supplying (101, 102) drive waveforms (DWk) to the pixels (Pij) to obtain during an image update period (IUk) an update of an image presented by the pixels (Pij), and

controlling (103) the driver (101, 102) to supply, during the image update period (IUk) wherein a particular optical transition of a particular one of the pixels (Pij) is required, an associated one of the drive waveforms (DWk) comprising a sequence of a

particular number of pulses (SPk), wherein consecutive ones of the pulses (SPk) of the sequence are separated by a separation period of time (SPT), the particular number of said pulses (SPk), and/or a duration of said pulses (SPk), and/or a duration of the separation period (SPT) of the associated one of the drive waveforms (DWk) being determined to obtain the particular optical transition at a desired energy of the drive waveform (DWk) during the image update period (IUk).

14. A display apparatus comprising a bi-stable display (100) and a drive circuit as claimed in claim1.

15. A display apparatus as claimed in claim 14, wherein the bi-stable display (100) is an electrophoretic display (1).